International Journal of Electrical and Electronics Engineering Research (IJEEER)
ISSN(P): 2250-155X; ISSN(O): 2278-943X
Vol. 3, Issue 5, Dec 2013, 101-114

A NOVEL PWM BASED MULTILEVEL CURRENT GENERATION USING INDUCTOR CELLS AND H-BRIDGE CURRENT-SOURCE INVERTER

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ABSTRACT

The recent development of new power semiconductor technologies capable of handling higher voltage and current ratings has helped the consolidation of multilevel topologies in medium-voltage & high voltage applications such as drive controlling, FACTS Controllers, HVDC systems etc. This paper presents a new circuit configuration of single-phase multilevel current-source inverter (CSI). In this new topology, a basic H-bridge CSI working as a main inverter generates a multilevel current waveform in cooperation with inductor cells connected in parallel as auxiliary circuits. The inductor -cells work generating the intermediate level currents to obtain a multilevel current waveform without additional external DC power sources. With this new topology, we can generate the multilevel current waveform from a single DC (Direct Current) power. The proposed circuit implemented by voltage degradation technique as well as PWM technique and results are obtained through Matlab/Simulink software package.

KEYWORDS: Current-Source Inverter (CSI), H-Bridge, Pulse Width Modulation (PWM), Inductor Cell, Multilevel

IINTRODUCTION

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Multilevel inverters have the capability to deliver higher output power with lower dv/dt or lower di/dt and with less-distorted output waveforms, resulting in reduction of electromagnetic interference (EMI) noise and size of an output filter [1]–[3]. Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources and drive applications.

Few topologies of the multilevel CSIs have been proposed by researchers and engineers. A conventional method to generate the multilevel current waveform is by paralleling some three-level H-bridge CSIs, as shown in Figure 1 [9]–[11]. This topology is a dual circuit of a cascade multilevel VSI [9]. However, the requirement of many isolated dc-

Current sources with their complex, bulky, and costly isolation transformers and inductors is a problem introduced by this configuration. Another topology of the multilevel CSI is obtained by applying a multicell topology of the CUSI (or multirating inductor multilevel CSI [9], which is a dual converter of a flying-capacitor-based full bridge multilevel VSI

[12]–[14]. However, this topology has a drawback with its bulky intermediate inductors and complexity for balancing control of the intermediate-level currents.

These converter topologies can generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental [5]. Although, in low-power applications, the switching frequency of the power switches is not restricted, a low switching frequency can increase the efficiency of the converter. Additionally, multilevel converters feature several dc links, making possible the independent voltage controls.

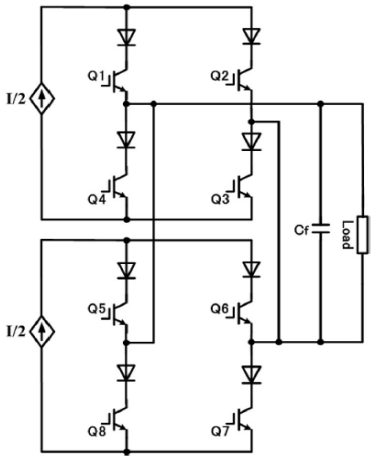

Figure 1: Parallel H-Bridge Five-Level CSI

This paper proposes a new circuit configuration of the multilevel CSI. In this new topology, a basic H-bridge CSI, working as a main inverter circuit, is connected in parallel with inductor cells working as auxiliary circuits. The inductor cells generate the intermediate levels of the multilevel output-current waveform, with no additional external dc-power sources [6] [7]. The operating performance of the proposed multilevel CSI is examined and is tested through some computer simulations. Furthermore, a laboratory experimental prototype of a five-level CSI circuit was set up to verify the proposed multilevel CSI topology.

CIRCUIT CONFIGURATION AND OPERATION

Operation of Proposed Multilevel CSI

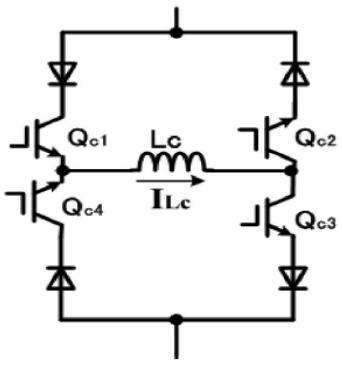

Figure 2: Proposed Inductor Cell Circuit

Figure 2 shows a configuration of the proposed inductor cell circuit composed by four unidirectional power switches Q_C1, Q_C2, Q_C3, and Q_C 4 , and an inductor L_C connected across the cell circuit. The newly proposed configuration of the multilevel CSI can be obtained by connecting the H-bridge CSI in parallel with a single or more inductor cells, as shown in a schematic diagram of the proposed multilevel CSI in Figure 3.

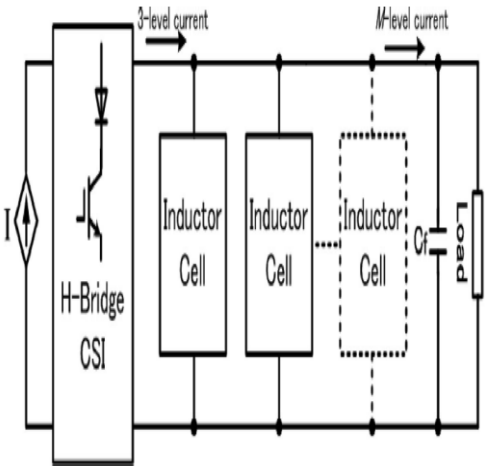

Figure 3: Proposed Configuration of Multilevel Csi

A five-level CSI configuration is obtained by connecting a single inductor cell, a nine-level CSI configuration is achieved by connecting two inductor cells in parallel with the main three-level H-bridge CSI, and so forth [8]. The relation between the level number of the output-current waveform (*M*) and the number of the inductor cells (*N*) can be formulated as follows:

$$M = 2^{(N+1)} + 1. \quad (1)$$

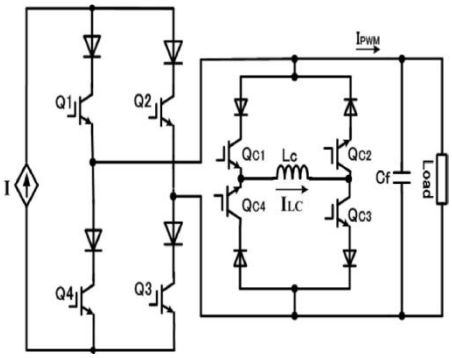

Figure 4: Proposed Five-Level CSI

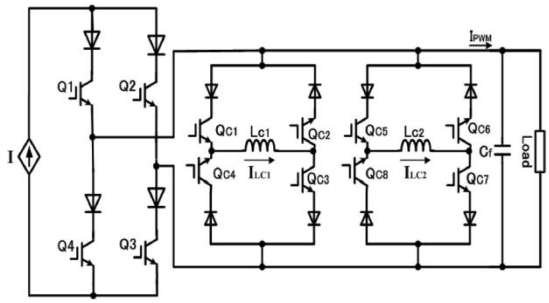

Figure 5: Proposed Nine-Level Csi

Figures 4 and 5 show the configurations of five-level and ninelevel CSIs using the proposed strategy, respectively. For *M*-level CSI, if the dc-current source of the main H-bridge CSI is assumed to have an amplitude *I*, the current flowing through the *N*th inductor cell *ILc* (*i*) is expressed as follows:

$$I_{L_c(i)} = \frac{I}{2^i}, \qquad \text{where} \qquad i = 1, 2, 3, \ldots, N. \quad (2)$$

The output-current levels of the five-level CSI are +*I*, +*I*/2, 0, −*I*/2, and −*I*. For the nine-level CSI, the output waveform has +*I*, +3*I*/4, +*I*/2, +*I*/4, 0, −*I*/4, −*I*/2, −3*I*/4, and –*I* current levels.

The inductor cells generate intermediate-level currents of the multilevel output waveform from the basic three-level current of the H-bridge CSI. It utilizes the charging and the discharging operation modes of the inductor. Figure 6 shows the operation modes of the inductor cell during a positive-cycle operation of the five-level CSI. The charging operation mode of the inductor *Lc* is conducted when the switches Q_C 1 and Q_C 3 are turned on, while the switches Q_C2 and Q_C 4 are turned off. A current I_{Lc} = *I*/2 flows through the power switches Q_C 1 and Q_C 3 that energizes the inductor *Lc* . The discharging operation mode is achieved by turning on the switchesQC 2 andQC 4 and by turning off Q_C 1 andQ_C 3 .The stored energy in the inductor is discharged to the load as a current *I*/2. The circulating current modes occur when the inductor cell deliver a null current to keep a constant current in the inductor cell. Similar operation modes occurred for the negative cycle of the output-current waveform [9] – [14]. Table I lists the switch states of the proposed five-level CSI. Power device utility and average switching frequency between Q_C 1, Q_C 2 and Q*C* 3, Q*C* 4 in the circulating modes of the inductor cell current is one of the considerations to use redundant switching states for *I*, 0, and −*I* output-current generation. It is also related to the heat distribution among the power switches Q*C* 1, Q*C* 2, Q*C* 3 and Q*C* 4 caused by the switching and conduction losses.

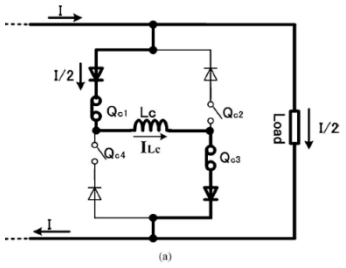

Figure (a)

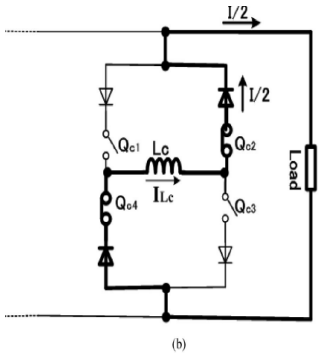

Figure (b)

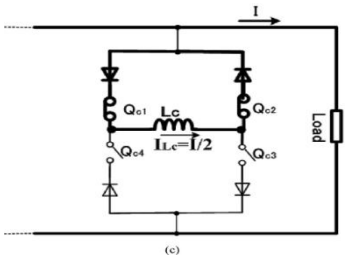

Figure (c)

Figure 6: Operation Modes of Inductor Cell. (a) Charging Mode of Inductor Cell. (b) Discharging Mode of Inductor Cell. (c) Circulating Current Mode of Inductor Cell

DC-Current Source

In the proposed multilevel CSI, the dc-current source is indispensable. In order to test the proposed multilevel CSI, the dc-current source is obtained by employing a chopper with a smoothing inductor (*Li*) connected with the H-bridge CSI. The chopper consists of a controlled switch (*QC*) that regulates the dc current flowing through the smoothing inductor as the dc input current *ILi*. A free-wheeling diode (*DF*) is used to keep continuous current flowing through the smoothing inductor. The chopper works as a regulated dc-current source. Figure 7 shows the five-level CSI configuration with the chopper-based dc-current source. The power source (*V*in) may be batteries system, photovoltaic (PV) modules, a fuel cell, or a rectifier.

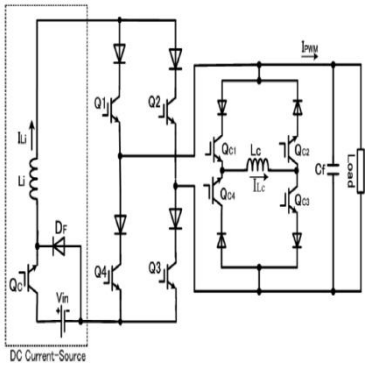

Figure 7: Proposed Five-Level CSI with Chopper Based Dc-Current Source

A simple proportional-integral (PI) regulator is applied to control the dc current flowing through the smoothing inductor, which determines the amplitude of the pulsewidth modulation (PWM) output-current waveform *I*PWM simultaneously. Making the smoothing inductor current follows the reference current is an objective of this current regulator [15]. The switching gate signals of the chopper switch (*Qc*) is generated by comparing the error signal of the detected inductor current in the steady state and a triangularwaveform after passing through the PI regulator.

PWM Technique and Inductor Cell Control

In order to achieve a lower distortion of the output-current

waveform, a PWM technique is applied. In this paper, a levelshifted multicarrier-based sinusoidal PWM technique is employed to generate gate signals for the CSI power switches and to obtain the PWM current waveforms [16], [17]. A schematic control diagram, including the current controller of the chopper and the inductor cell for the five-level CSI, is shown in Figure 8.

The control circuit of the inductor cell functions to control the operation modes, i.e., the charging, the discharging, and the circulating modes, of the inductor cell *Lc*.

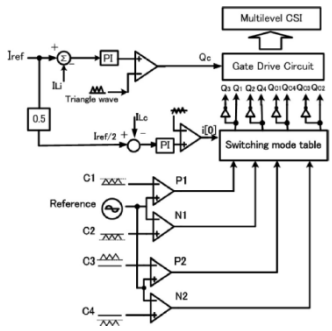

Figure 8: Control Diagram of Proposed Five-Level CSI

The current flowing through the inductor cell *ILc* is kept constant. It generates the intermediate-level currents based on the output-current waveform of the H-bridge CSI. A PI regulator is applied to zero the error between the detected current flowing through the inductor cell and the reference current to obtain stable and balanced intermediate-level currents. The amplitude of the inductor cell current is half of the dc input current *ILi*. The output of the PI regulator is modulated by a triangular carrier to generate the control signal *i*[0], determining the operation mode of the inductor

Cell. In case of the nine-level CSI, the control circuit of the second inductor cell is similar to the first inductor cell mentioned earlier. The difference is only the reference value of the second inductor cell current *ILc* 2, which is quarter of the dc input current. Therefore, for an*M*-level CSI, if the dc-current source is assumed to have amplitude *I*, the current flowing through the *N*th inductor cell *ILc* is as expressed in (2).

During the maximum and zero levels of the output-current generation, there is only circulating current mode, no charging and no discharging operation modes in the inductor cell, as listed in Table I. The frequency of the triangular carrier waveform determines the switching frequency of the inductor cell's power switches, which also regulates the charging and the discharging modes of the inductor cell. The discharging mode means that the inductor cell injects power to the load, and during the charging mode, the main H-bridge inverter injects power to the load. In case of a resistive load, the inductor cell value can be found as

$$L_c = \frac{I_{L_c} R}{f_s \Delta I_{L_c}} \tag{3}$$

where *ILc* is the inductor cell current (in amperes), *R* is a load resistance (in ohms), *fs* is a switching frequency of the inductor

Table 1: Switch States of Five – Level CSI

Q_1	Q_2	Q_3	Q_4	Q_{c1}	Q_{c2}	Q_{c3}	Q_{c4}	Output	Operation Mode of Inductor-Cell
1	0	1	0	1	1	0	0	+I	circulating mode
1	0	1	0	0	0	1	1	+I	circulating mode
1	0	1	0	1	0	1	0	+I/2	charging of inductor-cell
1	0	0	1	0	1	0	1	+I/2	discharging of inductor-cell
1	0	0	1	1	1	0	0	0	circulating mode
1	0	0	1	0	0	1	1	0	circulating mode
0	1	0	1	0	1	0	1	-I/2	charging of inductor-cell
0	1	1	0	1	0	1	0	-I/2	discharging of inductor-cell
0	1	0	1	0	0	1	1	-I	circulating mode
0	1	0	1	1	1	0	0	-I	circulating mode

Cell circuit (in hertz), andΔ*ILc* is an acceptable current ripple of the inductor cell current (in amperes). The higher the switching frequency is, the higher is the frequency of the charging and discharging of the inductor cell, which results in the smaller ripple of the inductor cell current, and even a smaller size of the inductor cell can be used.

Filter Capacitor

It is necessary to connect a capacitor across the load, because the inverter works as a current source and the load usually has an inductive component. The capacitor also functions to filter the harmonic components, e.g., switching harmonic components, of the PWM multilevel output current [18] [19]. The harmonic components of the PWM current will flow through the filter capacitor *Cf*. In general, using a higher switching frequency with its constraints, and using the higher level number of the output current, a smaller size of filter capacitor can be achieved.Aproper choice of the filter capacitor is also important to minimize the heat in the filter, such as capacitors having small equivalent series resistance (ESR).

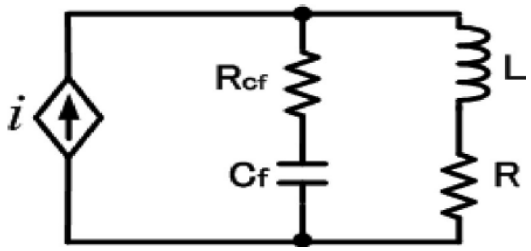

Figure 9: Simplified Model of CSI, Filter Capacitor, and Load

Table 2: Test Parameters

Smoothing inductor (Li) and inductor-cell (Lc)	1 mH and 5 mH
Power source voltage (Vin)	160 V
Inverter switching frequency	22 kHz
Filter capacitor C*f*	5 μF
Load	$R = 8\ \Omega$, L =1.2 mH
Output current frequency	60 Hz

Figure 9 shows a circuit model of the CSI (*i*) connected with a filter capacitor (*Cf)* with its internal resistance (*RCf)*, and the load, which is a series connection of a resistor *R* and an inductor *L*. For this circuit, the resonance frequency (ω0) is expressed as

$$\omega_0 = \frac{1}{\sqrt{LC_f}} \left[\frac{R^2 C_f - L}{R_{cf}^2 C_f - L} \right]^{1/2} \tag{4}$$

Therefore, the capacitor value that satisfies (4) should be avoided to prevent such resonance in the circuit. In addition, as in dual property with the VSI, because the inverter behaves as a current source, a capacitive load should be connected. Hence, the total impedance connected to the CSI including the filter capacitor should be a capacitive. It is another consideration in choosing the value of the filter capacitor.

MATLAB MODELEING AND SIMULATION RESULTS

In order to examine the proper operation of the proposed multilevel CSI topology, a five-level CSI configuration with chopper-based dc current source, were tested by using computer simulation with a Matlab/Simulink platform. The test parameters are listed in Table II.Here the simulation is carried out in two different cases 1). Proposed chopper based 5 & 9-Level CSI Configuration using Voltage Degradation Technique. 2). Proposed chopper based 5 & 9 -Level CSI Configuration using PWM Technique.

Case 1: Proposed Chopper based 5-Level CSI Configuration using Voltage Degradation Technique

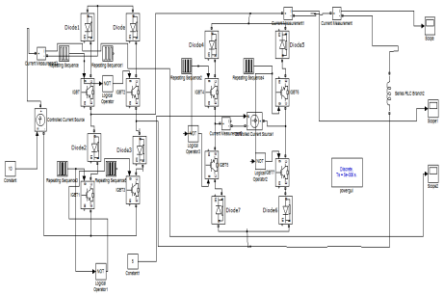

Figure 10: Matlab/Simulink Model of Proposed Chopper Based 5-Level CSI Configuration using Voltage Degradation Technique

Figure 10 shows the Matlab/Simulink Model of Proposed Chopper based 5-Level CSI Configuration using Voltage Degradation Technique using Matlab/Simulink Platform.

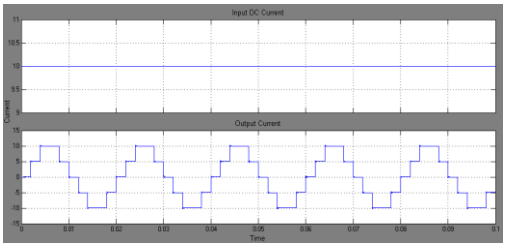

Figure 11: Input Current & Output Current

Figure 11 shows the Input Current & Output Current of Proposed Chopper based 5-Level CSI Configuration using Voltage Degradation Technique

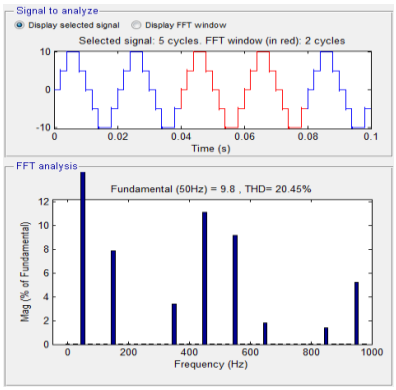

Figure 12: FFT Analysis of Output Current of Proposed Chopper Based 5-Level CSI Configuration using Voltage Degradation Technique

Figure 12 shows the FFT Analysis of Output Current of Proposed Chopper based 5-Level CSI Configuration using Voltage Degradation Technique; we get THD as 20.45%.

Case 2: Proposed Chopper based 5-Level CSI Configuration using Pulse Width Modulation (PWM) Technique.

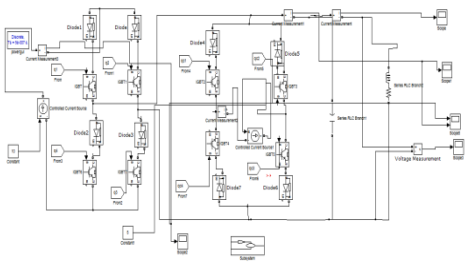

Figure 13: Matlab/Simulink Model of Proposed Chopper Based 5-Level CSI Configuration using PWM Technique

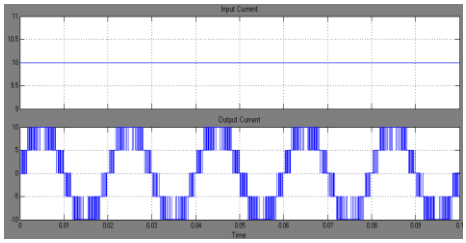

Figure 14: Input Current & Output Current

Figure 14 shows the Input Current & Output Current of Proposed Chopper based 5-Level CSI Configuration using PWM Technique.

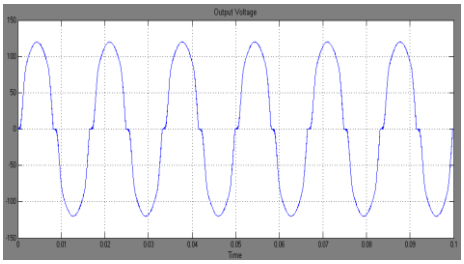

Figure 15: Output Voltage

Figure 15 shows the Output Voltage of Proposed Chopper based 5-Level CSI Configuration using PWM Technique.

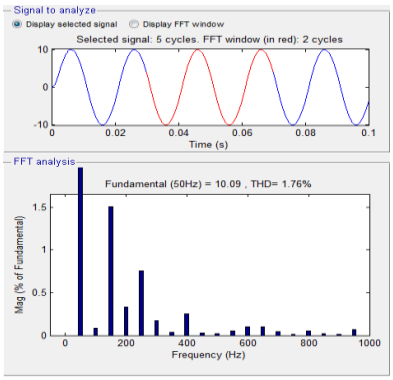

Figure 16: FFT Analysis of Output Current of Proposed Chopper Based 5-Level CSI Configuration using PWM Technique

Figure 16 shows the FFT Analysis of Output Current of Proposed Chopper based 5-Level CSI Configuration using PWM Technique; we get THD as 1.76%.

Case 3: Proposed Chopper based 9-Level CSI Configuration using Voltage Degradation Technique

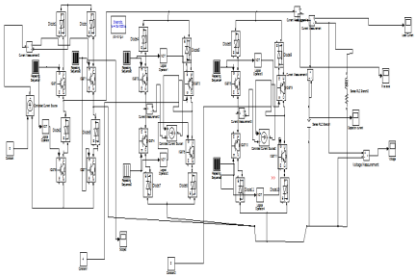

Figure 17: Matlab/Simulink Model of Proposed Chopper Based 9-Level CSI Configuration using Voltage Degradation Technique

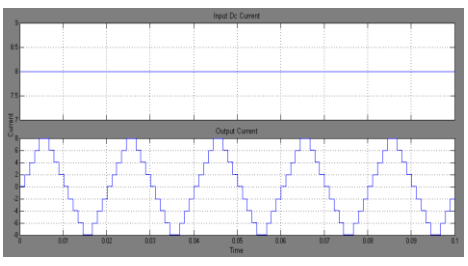

Figure 18: Input Current & Output Current

Figure 18 shows the Input Current & Output Current of Proposed Chopper based 9-Level CSI Configuration using Voltage Degradation Technique.

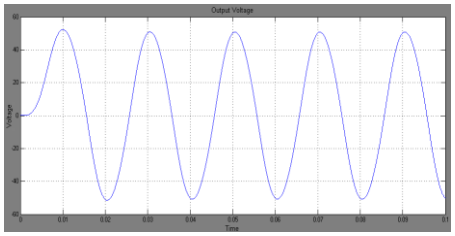

Figure 19: Output Voltage

Figure 19 shows the Output Voltage of Proposed Chopper based 9-Level CSI Configuration using Voltage Degradation Technique.

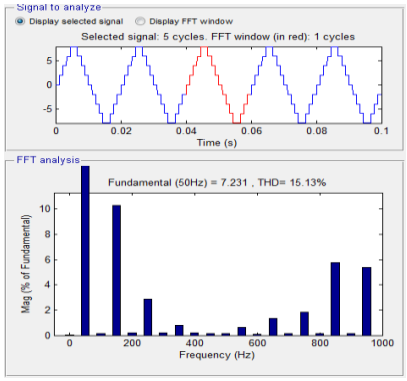

Figure 20: FFT Analysis of Output Current of Proposed Chopper Based 9-Level CSI Configuration using Voltage Degradation Technique

Figure 20 shows the FFT Analysis of Output Current of Proposed Chopper based 9-Level CSI Configuration using Voltage Degradation Technique; we get THD as 15.13%.

Case 4: Proposed Chopper based 9-Level CSI Configuration using Pulse Width Modulation (PWM) Technique.

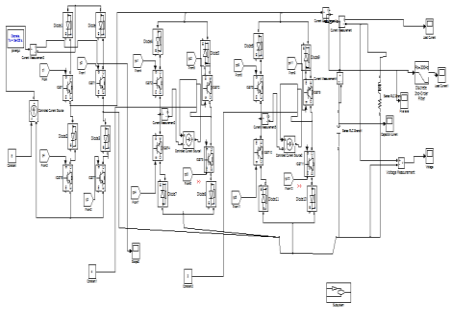

Figure 21: Matlab/Simulink Model of Proposed Chopper Based 9-Level CSI Configuration using PWM Technique

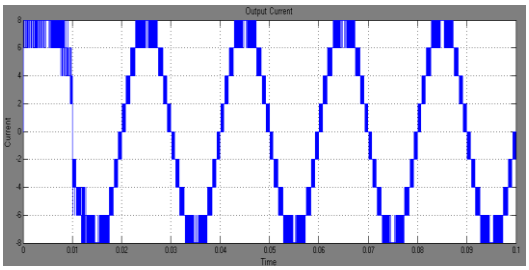

Figure 22: Output Current

Figure 22 shows the Output Current of Proposed Chopper based 9-Level CSI Configuration using PWM Technique.

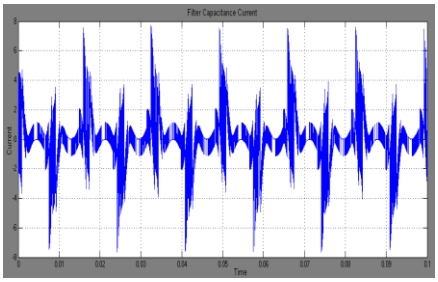

Figure 23: Filter Capacitor Current

Figure 23 shows the Filter Capacitor Current of Proposed Chopper based 9-Level CSI Configuration using PWM Technique.

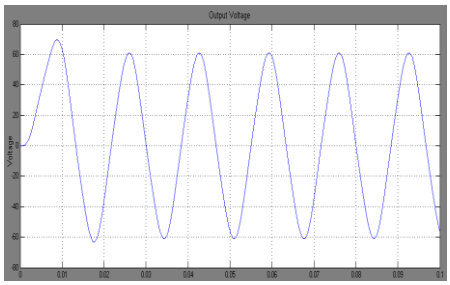

Figure 24: Output Voltage

Figure 24 shows the Output Voltage of Proposed Chopper based 9-Level CSI Configuration using Voltage Degradation Technique.

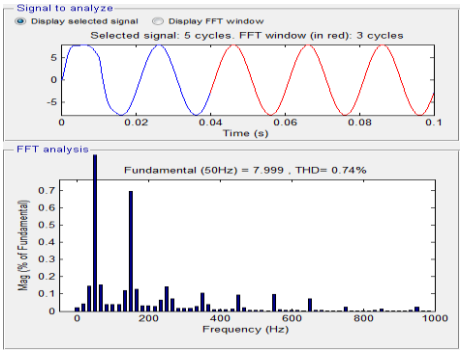

Figure 25: FFT Analysis of Output Current of Proposed Chopper Based 9-Level CSI Configuration using PWM Technique

Figure 25 shows the FFT Analysis of Output Current of Proposed Chopper based 9-Level CSI Configuration using PWM Technique; we get THD as 0.74%.

CONCLUSIONS

In this paper, a new configuration of 5 & 9 Level multilevel CSI implemented by voltage degradation technique as well as pwm technique which employs inductor cells as auxiliary circuit, has been proposed. The inductor cells are connected in parallel with the main H-bridge CSI to generate multilevel output-current waveforms without additional external dc-power sources. The following are some advantages that can be obtained using the proposed multilevel CSI topology compared with other topologies. Compared with the conventional two-level power converter, the proposed

multilevel CSI can generate multilevel output-current waveform with less distortion by connecting a single or more inductor cells across the H-bridge CSI. It results in a smaller *di/dt* produced by the circuit. Furthermore, a smaller size of the output capacitor filter can be used to filter the harmonic components of the output current. The control circuit of the intermediate-level current is simple, resulting in small size of the inductors. In conventional multilevel CSI, especially multi cell multilevel CSI topology and single-rating inductor multilevel CSI, they need bulky intermediate inductors with their control complexity to generate intermediate-level currents. By using the PWM technique instead of voltage degradation technique we get better THD values well in IEEE norms.

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